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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/759,715	01/13/2001	Hiroaki Tsugane	15.31/5631	2451

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EXAMINER
MAGEE, THOMAS J

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/759,715	Applicant(s) TSUGANE ET AL.	
	Examiner Thomas J. Magee	Art Unit 2811	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *5-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,15 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Claims 1 – 4, 15 and 16 in Letter No. 8 of January 19, 2002 is acknowledged.

Claim Rejections – 35 U.S.C. 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 – 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohyu et al. (US 6,291,847 B1) in view of Lee et al. (US 6,215,142 B1), Choi et al.(US 6,040,596) and Takada et al. (US 6,110,772)

Claims 1 – 4 recite a DRAM device with capacitor coupled with a capacitor and resistive element added in an analog region on the same substrate. Ohyu et al. disclose a DRAM device with capacitors for storing information contained in cells, but do not explicitly disclose an analog device on the same substrate. Lee et al.,Choi et al. and Takada et al. disclose the formation of capacitors and resistors as integral or peripheral elements in an IC or analog device. Takada et al. use ion implantation and diffusion to

adjust the doping (resistance) of layers in a semiconductor device (Col. 12, lines 23 – 39). Similarly, Choi et al. utilize ion imlantation to adjust sheet resistance of peripheral resistors in a DRAM device (Col. 8, lines 52 – 55). Lee et al. also disclose the formation of capacitors and interconnects for an analog device. In each case, methods of forming separate device elements, including capacitors and resistive elements, in DRAM, analog, or related devices have been disclosed in prior art. Further, it is well established in the art that certain process features can be "simultaneously" formed during a process sequence. For example, forming a cell plate and a resistance element simultaneously is relatively routine in processing. In like manner, formation of dielectric layers (simultaneously) in different locations is also well established within the art.

It would have been obvious to one of ordinary skill to simply combine Lee et al., Choi et al., and Takada et al. with Ohyu et al. to obtain a semiconductor device comprising: a DRAM including capacitor, with a capacitor and resistance element of an analog element on the same semiconductor substrate.

4. Claims 15 – 16 are rejected as unpatentable over Ohyu et al., as applied to Claims 1 – 4 above. As discussed previously, Ohyu et al. disclose formation of a DRAM device with capacitor elements, but do not disclose an analog device contained on the same substrate. Lee et al. disclose methods for forming capacitors and interconnects in analog devices, whereas Choi et al. disclose the formation of capacitors and peripheral

resistors in DRAM devices. Further, Takada et al. disclose methods of integrating capacitor and resistive elements in a semiconductor structure. Hence, it would have been obvious at the time of the invention to one of ordinary skill in the art to combine Lee et al., Choi et al., and Takada et al. with Ohyu et al. to obtain A DRAM structure including capacitor, with added analog elements containing capacitor and resistance elements on the same substrate.

Conclusions

5. Any inquiry concerning this or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(703) 305-5396**. The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Tom Thomas**, can be reached on **(703) 308-2772**. The fax number for the organization where this application or proceeding is assigned is **(703) 308-7722**.

Thomas Magee
June 25, 2002

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800